

S/N 10/643,585

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Steven L. Scott	Examiner:	Sheng Tsai
Serial No.:	10/643,585	Group Art Unit:	2186
Filed:	August 18, 2003	Docket:	1376.700US1
Title:	LATENCY TOLERANT DISTRIBUTED SHARED MEMORY MULTIPROCESSOR COMPUTER		

SUBMISSION OF FORMAL DRAWINGS

MS RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Replacement formal drawings for Figs. 1 through 12 (seven sheets) are submitted
herewith.

Respectfully submitted,

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Date July 8, 2008 By Thomas F. Brennan
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 8 day of July 2008.

CANDIS BUENDING

Name

Signature